

## MIXED SIGNAL MICROCONTROLLER

### FEATURES

- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode (AM):**  
All System Clocks Active
  - **Standby Mode (LPM3):**  
Real Time Clock With Crystal , Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:  
Low-Power Oscillator (VLO), General Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:
  - **Off Mode (LPM4):**  
Full RAM Retention, Supply Supervisor Operational, Fast Wake-Up:
  - **Shutdown Mode (LPM4.5)**
- **Wake-Up From Standby Mode**
- **16-Bit RISC Architecture, Extended Memory**
- **Flexible Power Management System**
  - **Fully Integrated LDO With Programmable Regulated Core Supply Voltage**
  - **Supply Voltage Supervision, Monitoring, and Brownout**
- **Unified Clock System**
  - **FLL Control Loop for Frequency Stabilization**
  - **Low-Power Low-Frequency Internal Clock Source (VLO)**
  - **Low-Frequency Trimmed Internal Reference Source (REFO)**
  - **32-kHz Watch Crystals (XT1)**
  - **High-Frequency Crystals Up to 32 MHz (XT2)**
- **16-Bit Timer TA0, Timer\_A With Five Capture/Compare Registers**
- **16-Bit Timer TA1, Timer\_A With Three Capture/Compare Registers**
- **16-Bit Timer TA2, Timer\_A With Three Capture/Compare Registers**
- **16-Bit Timer TB0, Timer\_B With Seven Capture/Compare Shadow Registers**
- **Two Universal Serial Communication Interfaces**
  - **USCI\_A0 and USCI\_A1 Each Supporting**
    - **Enhanced UART supporting Auto-Baudrate Detection**
    - **IrDA Encoder and Decoder**
    - **Synchronous SPI**
  - **USCI\_B0 and USCI\_B1 Each Supporting**
    - **I<sup>2</sup>C™**
    - **Synchronous SPI**
- **Integrated 3.3-V Power System**
- **12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature**
- **Comparator**
- **Hardware Multiplier Supporting 32-Bit Operations**
- **Serial Onboard Programming, No External Programming Voltage Needed**
- **Three Channel Internal DMA**
- **Basic Timer With Real-Time Clock Feature**

### DESCRIPTION

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in 3.5  $\mu$ s (typical).



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The MSP430F5326 is a microcontroller configuration with an integrated 3.3-V LDO, four 16-bit timers, a high-performance 12-bit analog-to-digital converter (ADC), two universal serial communication interfaces (USCI), hardware multiplier, DMA, real-time clock module with alarm capabilities, and 63 I/O pins. The MSP430F5326 includes all of these peripherals but has 47 I/O pins.

Typical applications include analog and digital sensor systems, data loggers and various general-purpose applications.

**ORDERING INFORMATION<sup>(1)</sup>**

| PRODUCT     | PACKAGE DESIGNATOR | PACKAGE                                | ORDERABLE PART NUMBER | PACKAGE QUANTITY |
|-------------|--------------------|----------------------------------------|-----------------------|------------------|
| MSP430F5326 | TD                 | Bare die in waffle pack <sup>(2)</sup> | MSP430F5326TDF1       | 49               |
|             |                    |                                        | MSP430F5326TDF2       | 10               |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Processing is per the Texas Instruments commercial production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.

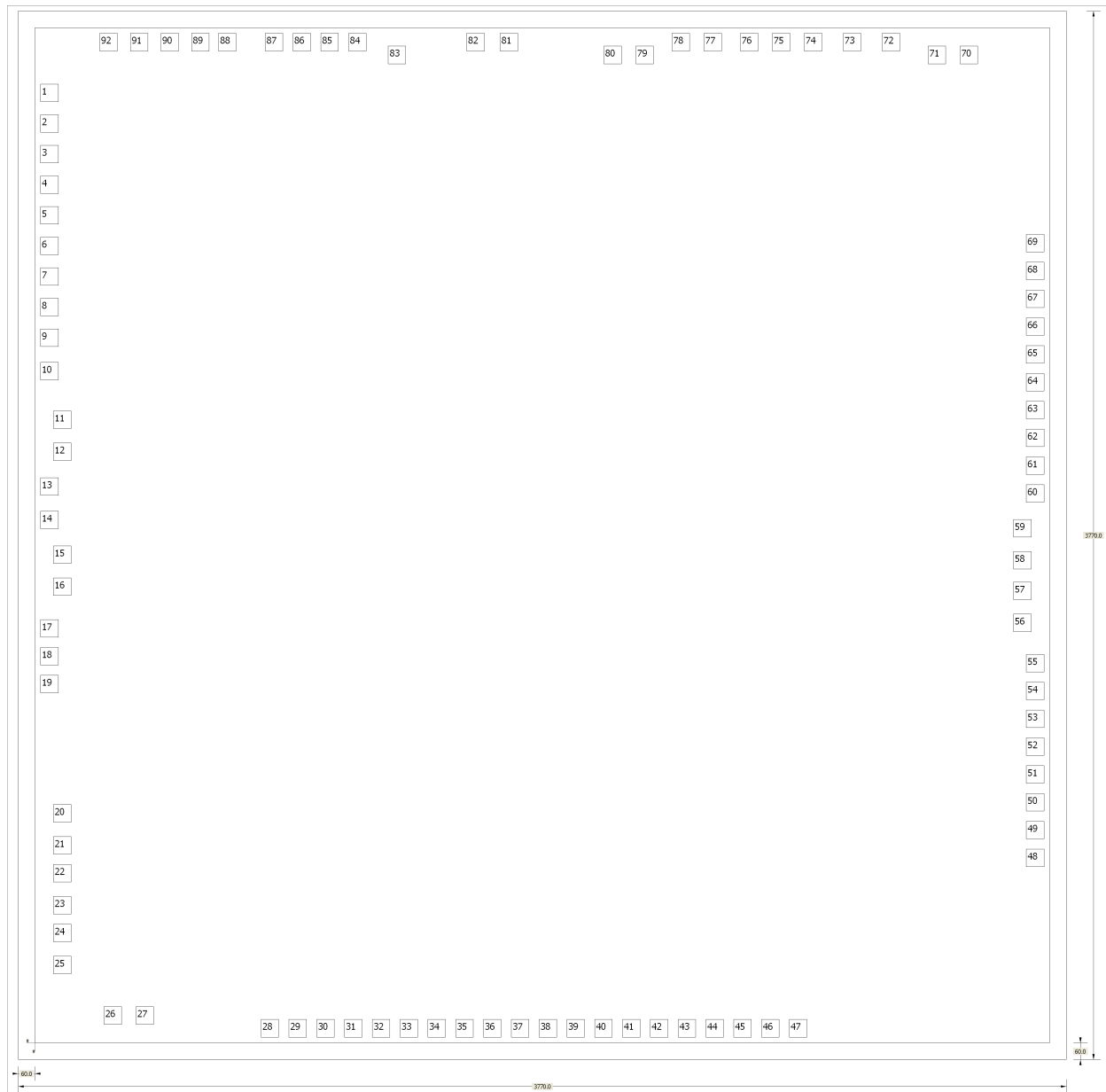


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## BARE DIE INFORMATION

| DIE THICKNESS | BACKSIDE FINISH        | BACKSIDE POTENTIAL | BOND PAD METALLIZATION COMPOSITION | BOND PAD THICKNESS |
|---------------|------------------------|--------------------|------------------------------------|--------------------|
| 11 mils.      | Silicon with backgrind | Floating           | W/TiW/AlCu (0.5%)/TiN              | 800 nm             |



**Table 1. Bond Pad Coordinates in Microns<sup>(1)</sup>**

| DESCRIPTION          | PAD NUMBER | X MIN | Y MIN    | X MAX | Y MAX    |
|----------------------|------------|-------|----------|-------|----------|
| P6.0/CB0/A0          | 1          | 19.8  | 3383     | 84.8  | 3447     |
| P6.1/CB1/A1          | 2          | 19.8  | 3273     | 84.8  | 3337     |
| P6.2/CB2/A2          | 3          | 19.8  | 3163     | 84.8  | 3227     |
| P6.3/CB3/A3          | 4          | 19.8  | 3053     | 84.8  | 3117     |
| P6.4/CB4/A4          | 5          | 19.8  | 2943     | 84.8  | 3007     |
| P6.5/CB5/A5          | 6          | 19.8  | 2833     | 84.8  | 2897     |
| P6.6/CB6/A6          | 7          | 19.8  | 2723     | 84.8  | 2787     |
| P6.7/CB7/A7          | 8          | 19.8  | 2613     | 84.8  | 2677     |
| P5.0/A8/VREF+/VeREF+ | 9          | 19.8  | 2503     | 84.8  | 2567     |
| P5.1/A9/VREF-/VeREF- | 10         | 19.8  | 2383     | 84.8  | 2447     |
| AVCC1                | 11         | 66.3  | 2208     | 131.3 | 2272     |
| AVCC1                | 12         | 66.3  | 2093     | 131.3 | 2157     |
| P5.4/XIN             | 13         | 19.8  | 1968     | 84.8  | 2032     |
| P5.5/XOUT            | 14         | 19.8  | 1848     | 84.8  | 1912     |
| AVSS1                | 15         | 66.3  | 1722.995 | 131.3 | 1786.995 |
| AVSS1                | 16         | 66.3  | 1607.995 | 131.3 | 1671.995 |
| N/C                  | 17         | 19.8  | 1458     | 84.8  | 1522     |
| N/C                  | 18         | 19.8  | 1358     | 84.8  | 1422     |
| N/C                  | 19         | 19.8  | 1258     | 84.8  | 1322     |
| DVCC1                | 20         | 66.3  | 793      | 131.3 | 857      |
| DVCC1                | 21         | 66.3  | 678      | 131.3 | 742      |
| DVSS1                | 22         | 66.3  | 578      | 131.3 | 642      |
| DVSS1                | 23         | 66.3  | 463      | 131.3 | 527      |
| N/C                  | 24         | 66.3  | 363      | 131.3 | 427      |
| N/C                  | 25         | 66.3  | 248      | 131.3 | 312      |
| VCORE                | 26         | 248   | 66.3     | 312   | 131.3    |
| VCORE                | 27         | 363   | 66.3     | 427   | 131.3    |
| P1.0/TA0CLK/ACLK     | 28         | 813   | 19.8     | 877   | 84.8     |
| P1.1/TA0.0           | 29         | 913   | 19.8     | 977   | 84.8     |
| P1.2/TA0.1           | 30         | 1013  | 19.8     | 1077  | 84.8     |
| P1.3/TA0.2           | 31         | 1113  | 19.8     | 1177  | 84.8     |
| P1.4/TA0.3           | 32         | 1213  | 19.8     | 1277  | 84.8     |
| P1.5/TA0.4           | 33         | 1313  | 19.8     | 1377  | 84.8     |
| P1.6/TA1CLK/CBOUT    | 34         | 1413  | 19.8     | 1477  | 84.8     |
| P1.7/TA1.0           | 35         | 1513  | 19.8     | 1577  | 84.8     |
| N/C                  | 36         | 1613  | 19.8     | 1677  | 84.8     |
| N/C                  | 37         | 1713  | 19.8     | 1777  | 84.8     |
| N/C                  | 38         | 1813  | 19.8     | 1877  | 84.8     |
| N/C                  | 39         | 1913  | 19.8     | 1977  | 84.8     |
| N/C                  | 40         | 2013  | 19.8     | 2077  | 84.8     |
| P2.0/TA1.1           | 41         | 2113  | 19.8     | 2177  | 84.8     |
| P2.1/TA1.2           | 42         | 2213  | 19.8     | 2277  | 84.8     |
| P2.2/TA2CLK/SMCLK    | 43         | 2313  | 19.8     | 2377  | 84.8     |
| P2.3/TA2.0           | 44         | 2413  | 19.8     | 2477  | 84.8     |
| P2.4/TA2.1           | 45         | 2513  | 19.8     | 2577  | 84.8     |
| P2.5/TA2.2           | 46         | 2613  | 19.8     | 2677  | 84.8     |

(1) Substrate V<sub>DD</sub>.

**Table 1. Bond Pad Coordinates in Microns<sup>(1)</sup> (continued)**

| DESCRIPTION                 | PAD NUMBER | X MIN   | Y MIN  | X MAX   | Y MAX  |
|-----------------------------|------------|---------|--------|---------|--------|
| P2.6/RTCCLK/DMAE0           | 47         | 2713    | 19.8   | 2777    | 84.8   |
| P2.7/UCB0STE/UCA0CLK        | 48         | 3565.2  | 633    | 3630.2  | 697    |
| P3.0/UCB0SIMO/UCB0SDA       | 49         | 3565.2  | 733    | 3630.2  | 797    |
| P3.1/UCB0SOMI/UCB0SCL       | 50         | 3565.2  | 833    | 3630.2  | 897    |
| P3.2/UCB0CLK/UCA0STE        | 51         | 3565.2  | 933    | 3630.2  | 997    |
| P3.3/UCA0TXD/UCA0SIMO       | 52         | 3565.2  | 1033   | 3630.2  | 1097   |
| P3.4/UCA0RXD/UCA0SOMI       | 53         | 3565.2  | 1133   | 3630.2  | 1197   |
| N/C                         | 54         | 3565.2  | 1233   | 3630.2  | 1297   |
| N/C                         | 55         | 3565.2  | 1333   | 3630.2  | 1397   |
| DVSS2                       | 56         | 3518.7  | 1478   | 3583.7  | 1542   |
| DVSS2                       | 57         | 3518.7  | 1593   | 3583.7  | 1657   |
| DVCC2                       | 58         | 3518.7  | 1703   | 3583.7  | 1767   |
| DVCC2                       | 59         | 3518.7  | 1818   | 3583.7  | 1882   |
| N/C                         | 60         | 3565.2  | 1943   | 3630.2  | 2007   |
| N/C                         | 61         | 3565.2  | 2043   | 3630.2  | 2107   |
| P4.0/PM_UCB1STE/PM_UCA1CLK  | 62         | 3565.2  | 2143   | 3630.2  | 2207   |
| P4.1/PM_UCB1SIMO/PM_UCB1SDA | 63         | 3565.2  | 2243   | 3630.2  | 2307   |
| P4.2/PM_UCB1SOMI/PM_UCB1SCL | 64         | 3565.2  | 2343   | 3630.2  | 2407   |
| P4.3/PM_UCB1CLK/PM_UCA1STE  | 65         | 3565.2  | 2443   | 3630.2  | 2507   |
| P4.4/PM_UCA1TXD/PM_UCA1SIMO | 66         | 3565.2  | 2543   | 3630.2  | 2607   |
| P4.5/PM_UCA1RXD/PM_UCA1SOMI | 67         | 3565.2  | 2643   | 3630.2  | 2707   |
| P4.6/PM_NONE                | 68         | 3565.2  | 2743   | 3630.2  | 2807   |
| P4.7/PM_NONE                | 69         | 3565.2  | 2843   | 3630.2  | 2907   |
| VSSU                        | 70         | 3327.17 | 3518.7 | 3391.17 | 3583.7 |
| VSSU                        | 71         | 3212.17 | 3518.7 | 3276.17 | 3583.7 |
| PU.0                        | 72         | 3047.17 | 3565.2 | 3111.17 | 3630.2 |
| N/C                         | 73         | 2907.17 | 3565.2 | 2971.17 | 3630.2 |
| PU.1                        | 74         | 2767.17 | 3565.2 | 2831.17 | 3630.2 |
| LDO1                        | 75         | 2652.17 | 3565.2 | 2716.17 | 3630.2 |
| LDO1                        | 76         | 2537.17 | 3565.2 | 2601.17 | 3630.2 |
| LDO0                        | 77         | 2405.67 | 3565.2 | 2469.67 | 3630.2 |
| LDO0                        | 78         | 2290.67 | 3565.2 | 2354.67 | 3630.2 |
| N/C                         | 79         | 2160.67 | 3518.7 | 2224.67 | 3583.7 |
| AVSS2                       | 80         | 2045.67 | 3518.7 | 2109.67 | 3583.7 |
| P5.2/XT2IN                  | 81         | 1673    | 3565.2 | 1737    | 3630.2 |
| P5.3/XT2OUT                 | 82         | 1553    | 3565.2 | 1617    | 3630.2 |
| TEST/SBWTK                  | 83         | 1270.5  | 3518.7 | 1334.5  | 3583.7 |
| PJ.0/TDO                    | 84         | 1128    | 3565.2 | 1192    | 3630.2 |
| PJ.1/TDI/TCLK               | 85         | 1028    | 3565.2 | 1092    | 3630.2 |
| 62.PJ.2/TMS                 | 86         | 928     | 3565.2 | 992     | 3630.2 |
| 63.PJ.3/TCK                 | 87         | 828     | 3565.2 | 892     | 3630.2 |
| 64.RST/NMI/SBWTDIO          | 88         | 660.5   | 3565.2 | 724.5   | 3630.2 |
| N/C                         | 89         | 563     | 3565.2 | 627     | 3630.2 |

**Table 1. Bond Pad Coordinates in Microns<sup>(1)</sup> (continued)**

| DESCRIPTION | PAD NUMBER | X MIN | Y MIN  | X MAX | Y MAX  |
|-------------|------------|-------|--------|-------|--------|
| N/C         | 90         | 453   | 3565.2 | 517   | 3630.2 |
| N/C         | 91         | 343   | 3565.2 | 407   | 3630.2 |
| N/C         | 92         | 233   | 3565.2 | 297   | 3630.2 |

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/ Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|-------------------|------------------------------|--------------------------|
| MSP430F5326TDF1  | ACTIVE                |              |                 | 0    | 49          | TBD                     | Call TI           | N / A for Pkg Type           |                          |
| MSP430F5326TDF2  | ACTIVE                |              |                 | 0    | 10          | TBD                     | Call TI           | N / A for Pkg Type           |                          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### Applications

|                               |                                                                                          |
|-------------------------------|------------------------------------------------------------------------------------------|
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| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
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